



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,751	02/09/2001	Toshio Yamada	60188-028	5852

7590 01/29/2004

Michael E. Fogarty  
McDermott, Will & Emery  
600 13th Street, N.W.  
Suite 1200  
Washington, DC 20005-3096

EXAMINER

VO, LILIAN

ART UNIT	PAPER NUMBER
----------	--------------

2127

DATE MAILED: 01/29/2004

9

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/779,751

Applicant(s)

YAMADA, TOSHIO

Examiner

Lilian Vo

Art Unit

2127

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 November 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 6, 8 - 11 and 21 - 24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6, 8 - 11 and 21 - 24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2, 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. Claims 6, 8 – 11 and 21 – 24 are pending. Claims 1 – 5, 7 and 12 – 20 have been canceled.
2. Applicant need to update the status of application serial number 09/102,166 with the US patent number.

#### *Claim Objections*

3. **Claims 21 and 22** are objected to because of the following informalities. Claims 21 and 22 recite as depending on claim 10 or 13. However, claim 13 has been cancelled and has not been further treated on the merits.

Appropriate correction is required.

#### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:  
  
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.  
  
**Claim 8** recites the limitation "the same area" in page 3, lines 3. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 6 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Saito et al. (US 5,968,160, hereinafter Saito).

8. Regarding **claim 6**, Saito teaches the invention as claimed including a data processing method comprising the steps of:

writing a processing specification information in a first area corresponding to a first word line within a semiconductor device comprising at least one memory array and a data processor to said at least one memory array through at least one internal data bus (fig. 2, B1, col. 10, lines 4 – 6, 19 – 23, 35 – 40);

writing data to be processed in a second area corresponding to a second word line, which is different from the first word line, within said semiconductor device (fig. 2, B2, col. 10, lines 4 – 6, 28 – 35);

transferring said processing specification information through said at least one internal data bus to said data processor (fig. 2, b1, A2, col. 10, lines 7 – 13);

Art Unit: 2127

transferring said data through said at least one internal data bus to said data processor (fig. 2, b4, A3, col. 9, line 64 – col. 10, lines 49);

processing said data by said data processor using said processing specification information and writing resultant processed data through said at least one internal data bus in a third area corresponding to a third word line within said semiconductor device (fig. 2, 3-B, col. 11, lines 30 - 55); and

obtaining said resultant processed data by reading said third area after writing said resultant processed data (col. 11, line 31 – col. 12, line 48).

9. Regarding **claim 24**, Saito discloses the data processing method of claim 6, wherein said data processor comprises a first data processor portion, a second data processor portion and a register coupled between said first and second data processor portions (fig. 2, A2 and A 3, and fig. 3, A2, A3, D1 – D4, col. 8, lines 7 – 36).

### ***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2127

11. Claims 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 5,968,160, hereinafter Saito) as applied to claims 6 above, in view of Van Doren et al. (US 5,761,731, hereafter referred to Van Doren).

12. Regarding **claim 8**, although Saito discloses the data processing method of claim 6, he did not teach the second area and third area are the same area and that the resultant processed data is overwritten in the second area. Nevertheless, Van Doren teaches of the processing data and the resultant processed data areas are of the same area and that the resultant processed data are being overwritten in the second area of the memory (col. 9, lines 46 – 53).

13. It would have been obvious for one of ordinary skill in the art, at the time the invention was made to combine the teachings of Saito and Van Doren because Van Doren's feature of using same area would guarantee data coherency in a system where multiple nodes require atomic transactions (col. 3, lines 21 – 23).

14. Regarding **claim 11**, although Saito discloses the data processing method of claim 6, except the additional limitation as claimed. Nevertheless, Van Doren discloses a data processing system, in which immediately before executing said processing by said semiconductor device having the data processing function, information describing said processing to be executed is dynamically rewritten for executing said processing (col. 9, lines 45 – 58 and fig. 4).

15. It would have been obvious for one of ordinary skill in the art, at the time the invention was made to incorporate these features of Van Doren's invention to Saito's system to guarantee

Art Unit: 2127

data coherency in a system where multiple nodes require atomic transactions (col. 3, lines 21 – 23).

16. Claims 9, 10 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 5,968,160, hereinafter Saito) as applied to claim 6 above, in view of Satou et al. (US 5,717,946, hereafter referred to Satou).

17. Regarding **claim 9**, although Saito discloses the data processing method of claim 6, except the additional limitation as claimed. Nevertheless, Satou discloses a data processing system wherein said controller reads time information required for said processing to be executed (col. 42, lines 39 – 61, col. 47, lines 4 – 63 and col. 49, lines 9 – 33, and fig. 38, 39 and 44), and reads said resultant processed data written in said third area on the basis of said read time information after time corresponding to said time information elapses (col. 42, lines 23 – 46).

18. It would have been obvious for one of ordinary skill in the art, at the time the invention was made to incorporate the feature in Satou's system to Saito's invention so that the instructions are processed as high speed by burst transferred between a CPU and a memory (col. 1, lines 11 – 13).

19. Regarding **claim 10**, Saito failed to teach the feature of storing time information required for each processing to be executed by the semiconductor device. Nevertheless, Satou discloses a

Art Unit: 2127

data processing system with a table that stores time information required for each processing to be executed (fig. 44).

20. It would have been obvious for one of ordinary skill in the art, at the time the invention was made to incorporate this feature to Saito's invention to enhance the system performance with the provided timing information.

21. Regarding **claim 22**, Saito discloses the data processing system method of claim 10, wherein said memory network has a bus structure (fig. 2).

22. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 5,968,160, hereinafter Saito) in view of Satou et al. (US 5,717,946, herein after Satou) as applied to claims 6, 9 – 10 above, and further in view of Sandberg (US 5,592,625).

23. Regarding **claim 21**, Saito and Satou failed to teach the memory network has a ring network structure. However, Sandberg teaches the memory network with a ring network structure (col. 3, line 54 – col. 4, line 7).

24. Therefore, it would have been obvious for one of ordinary skill in the art, at the time the invention was made to incorporate a ring network structure to the combined system of Saito and Satou because it will span larger distance in their network.



Art Unit: 2127

25. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 5,968,160, hereinafter Saito) as applied to claim 6 above, in view of Leach et al. (US 5,179,689, herein after Leach).

26. Regarding **claim 23**, Saito failed to teach that the data processor comprises reconfigurable logic. Nevertheless, Leach discloses of a data processor that can be reconfigured dynamically (col. 25, lines 10 – 15).

27. It would have been obvious for one of ordinary skill in the art, at the time the invention was made to incorporate this feature to Saito's system to have a system that would allow the user to optimize microcomputer based upon the desired application (col. 25, lines 15 – 18).

### ***Response to Arguments***

28. Applicant's amendments filed on 11/13/03 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Davies, US 5,450,603 disclosed SIMD system connected to bus.

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2127

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

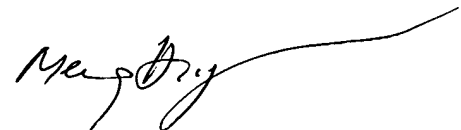
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 703-305-7864. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 703-305-9678. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Lilian Vo  
Examiner  
Art Unit 2127

lv  
January 20, 2004



**MENG-AL T. AN**  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100